What is claim d is:

1. A logic circuit test apparatus for testing a logic circuit having a plurality of input terminals and a plurality of output terminals by inputting original test signals to the input terminals of the logic circuit and testing output signals from the output terminals of the logic circuit, the logic circuit test apparatus comprising:

a common test signal generating circuit which groups the input terminals of the logic circuit on the basis of logic states of original test signals to be applied to the respective input terminals of the logic circuit and outputs common test signals from common test signal output terminals thereof smaller in number than the input terminals of the logic circuit;

an input connection switching circuit which switches connections of the common test signal output terminals of the common test signal generating circuit with the input terminals of the logic circuit so as to convert the common test signals into the original test signals and apply the original test signals to the input terminals of the logic circuit;

a common expected signal generating circuit which groups the output terminals of the logic circuit on the basis of logic states of expected signals to be outputted from the respective output terminals of the logic circuit in association with the original test signals and outputs common expected signals from expected signal output terminals thereof smaller in number than the output

terminals of the logic circuit;

an output connection switching circuit which switches connections of the output terminals of the logic circuit with output signal measurement terminals provided in a one-to-one correspondence with the expected signal output terminals of the common expected signal generating means so as to compare the output signals outputted from the respective output terminals of the logic circuit with the common expected signals; and

a connection switching control circuit for synchronously controlling the input connection switching circuit and the output connection switching circuit.

2. A logic circuit test apparatus for testing a logic circuit having a plurality of input terminals and a plurality of output terminals by inputting original test signals to the input terminals of the logic circuit and testing output signals from the output terminals of the logic circuit, the logic circuit test apparatus comprising:

a common test signal generating circuit which groups the input terminals of the logic circuit on the basis of logic states of original test signals to be applied to the respective input terminals of the logic circuit and outputs common test signals from common test signal output terminals thereof smaller in number than the input terminals of the logic circuit; and

an input connection switching circuit which switches connections of the common test signal output terminals of the

common test signal generating circuit with the input terminals of the logic circuit so as to convert the common test signals into the original test signals and apply the original test signals to the respective input terminals of the logic circuit.

3. A logic circuit test apparatus as set forth in claim 2, wherein the common test signal generating circuit groups the input terminals on the basis of the logic states of the original test signals and logic states of inverted signals obtained by logic inversion of the original test signals to generate the common test signals.

4. A logic circuit test apparatus as set forth in claim 2, wherein the input connection switching circuit comprises an input connection switching information memory for switching the connections, the memory storing therein input connection switching information necessary for switching the connections of the common test signal output terminals of the common test signal generating circuit with the input terminals of the logic circuit.

5. A logic circuit test apparatus for testing a logic circuit having a plurality of input terminals and a plurality of output terminals by inputting original test signals to the input terminals of the logic circuit and testing output signals from the output terminals of the logic circuit, the logic circuit test apparatus comprising:

a common expected signal generating circuit which groups

the output terminals of the logic circuit on the basis of logic states of expected signals to be outputted from the respective output terminals of the logic circuit in association with the original test signals and outputs common expected signals from expected signal output terminals thereof smaller in number than the output terminals of the logic circuit; and

an output connection switching circuit which switches connections of the output terminals of the logic circuit with output signal measurement terminals provided in a one-to-one correspondence with the expected signal output terminals of the common expected signal generating circuit so as to compare the output signals outputted from the respective output terminals of the logic circuit with the common expected signals.

6. A logic circuit test apparatus as set forth in claim 5, wherein the common expected signal generating circuit groups the output terminals of the logic circuit on the basis of the logic states of the expected signals and logic states of inverted expected signals obtained by logic inversion of the expected signals to generate the common expected signals.

7. A logic circuit test apparatus as set forth in claim 5, wherein the output connection switching circuit comprises an output connection switching information memory for switching the connections, the memory storing therein output connection switching information necessary for switching the connections of the output terminals of the logic circuit with the output signal

measurement terminals.

8. A logic circuit test method for testing a logic circuit having a plurality of input terminals and a plurality of output terminals by inputting original test signals to the input terminals of the logic circuit and testing output signals from the output terminals of the logic circuit, the logic circuit test method comprising the steps of:

grouping the input terminals of the logic circuit on the basis of logic states of original test signals to be applied to the respective input terminals of the logic circuit, further grouping the grouped input terminals on the basis of logic states of the original test signals in the next cycle period, and sequentially repeating the grouping of the input terminals until the number of input terminal groups exceeds the number of common test signal output terminals of a common test signal generating circuit smaller than the number of the input terminals of the logic circuit so as to output common test signals from the common test signal output terminals of the common test signal generating circuit; and

when the number of the groups exceeds the number of the common test signal output terminals of the common test signal generating circuit, generating the common test signals for corresponding respective input terminal groups provided immediately before the last grouping to the common test signal output terminals of the common test signal generating circuit.

9. A logic circuit test method as set forth in claim 8, wherein the common test signal generating circuit groups the input

terminals on the basis of the logic states of the original test signals and logic states of inverted signals obtained by logic inversion of the original test signals, repeats the grouping until the number of input terminal groups exceeds a number twice the number of the common test signal output terminals of the common test signal generating circuit and, when the number of the groups exceeds the number twice the number of the common test signal output terminals of the common test signal generating circuit, generates the common test signals for corresponding respective input terminal groups obtained by removing equivalent groups from input terminal groups provided immediately before the last grouping to the common test signal output terminals of the common test signal generating circuit.

10. A logic circuit test method for testing a logic circuit having a plurality of input terminals and a plurality of output terminals by inputting original test signals to the input terminals of the logic circuit and testing output signals from the output terminals of the logic circuit, the logic circuit test method comprising the steps of:

grouping the output terminals of the logic circuit on the basis of logic states of expected signals to be outputted from the respective output terminals of the logic circuit in association with the original test signals, further grouping the grouped output terminals on the basis of logic states of the expected signals in the next cycle period, and sequentially repeating the grouping of the output terminals until the number of output terminal groups

exceeds the number of expected signal output terminals of a common expected signal generating circuit smaller than the number of the output terminals of the logic circuit so as to output common expected signals from the expected signal output terminals of the common expected signal generating circuit; and

when the number of the groups exceeds the number of the expected signal output terminals of the common expected signal generating circuit, generating the common expected signals for corresponding respective output terminal groups provided immediately before the last grouping to the expected signal output terminals of the common expected signal generating circuit.

11. A logic circuit test method as set forth in claim 10, wherein the common expected signal generating circuit groups the output terminals of the logic circuit on the basis of the logic states of the expected signals and logic states of inverted signals obtained by logic inversion of the expected signals, sequentially repeats the grouping until the number of output terminal groups exceeds a number twice the number of the expected signal output terminals of the common expected signal generating circuit and, when the number of the groups exceeds the number twice the number of the expected signal output terminals of the common expected signal generating circuit, generates the common expected signals for corresponding output terminal groups obtained by removing equivalent groups from output terminal groups provided immediately before the last grouping to the expected signal output

terminals of the common expected signal generating circuit.

12. A logic circuit test method for testing a logic circuit having a plurality of input terminals and a plurality of output terminals by inputting original test signals to the input terminals of the logic circuit and testing output signals from the output terminals of the logic circuit, the logic circuit test method comprising the steps of:

grouping the input terminals of the logic circuit on the basis of logic states of original test signals to be applied to the input terminals of the logic circuit, further grouping the grouped input terminals on the basis of logic states of the original test signals in the next cycle period, and sequentially repeating the grouping of the input terminals until the number of input terminal groups exceeds the number of common test signal output terminals of a common test signal generating circuit smaller than the number of the input terminals of the logic circuit so as to output common test signals from the common test signal output terminals of the common test signal generating circuit;

when the number of the groups exceeds the number of the common test signal output terminals of the common test signal generating circuit, generating the common test signals for corresponding respective input terminal groups provided immediately before the last grouping to the common test signal output terminals of the common test signal generating circuit;

grouping the output terminals of the logic circuit on the basis of logic states of expected signals to be outputted from the

respective output terminals of the logic circuit in association with the original test signals, further grouping the grouped output terminals on the basis of logic states of the expected signals in the next cycle period, and sequentially repeating the grouping of the output terminals until the number of output terminal groups exceeds the number of expected signal output terminals of a common expected signal generating circuit smaller than the number of the output terminals of the logic circuit so as to output common expected signals from the expected signal output terminals of the common expected signal generating circuit; and

when the number of the groups exceeds the number of the expected signal output terminals of the common expected signal generating circuit, generating the common expected signals for corresponding respective output terminal groups provided immediately before the last grouping to the expected signal output terminals of the common expected signal generating circuit.